

Energy Efficient and Process Tolerant Full Adder in Technologies beyond CMOS

Aminul Islam¹, Member, IEEE, M. W. Akram², Mohd. Hasan², Member, IEEE

¹Department of Electronics and Communication Engineering,

Birla Institute of Technology (deemed university), Mesra, Ranchi, Jharkhand, India

E-mail: aminulislam@bitmesra.ac.in

²Department of Electronics Engineering, Zakir Husain College of Engineering and Technology

Aligarh Muslim University, Aligarh, U.P., India

E-mail: akrammw@gmail.com

Abstract—This paper presents 1-bit full adder cell in emerging technologies like FinFET and CNFET that operates in the moderate inversion region for energy efficiency, robustness and higher performance. The performance of the adder is improved by the optimum selection of important process parameters like oxide and fin thickness in FinFET and number of carbon nanotubes, chirality vector and pitch in CNFET. The optimized CNFET-based full adder (OP-CNFET) has higher speed, lower PDP (power-delay product) and lower power dissipation as compared to the MOSFET and FinFET full adder cells. The OP-CNFET design also offers tight spread in power, delay and PDP variability against process, voltage and temperature variations. All the evaluations have been carried out using HSPICE simulations based on 32 nm BPTM (Berkeley Predictive Technology Model).

Index Terms—Variability, power-delay product (PDP), moderate inversion region (MIR), optimized FinFET-based full adder (OP-FinFET), optimized CNFET-based full adder (OP-CNFET).

I. INTRODUCTION

Addition is the most commonly used arithmetic operation in microelectronic systems and it is often one of the speed-limiting elements [1]. Hence, the optimization of the adder both in terms of speed and/or power consumption should be pursued. It is necessary to improve the performance of full adder cell for fast and low energy operations of arithmetic block. In the last five years it has been demonstrated that operating the device at minimum energy point (MEP) gives large penalty in delay, where as minimum energy delay point (MEDP) gives better circuit performance in terms of delay as well as energy and turn out to be the center of attraction for the researchers. However, there is a new class of circuit applications which demands for ultra low energy consumption with moderate throughput. These circuits must be operated at minimum energy point to achieve energy at ultra low level. This represents an important mind-shift: rather than starting out from a design optimized for maximum performance. The initial design point is now the minimum-energy one. It has been shown that for most of the digital circuit's minimum energy point occurs in the subthreshold operational region of the MOS transistors [2], [3]. However, performance degradation due to minute leakage current as drive current and more sensitivity for process variation due to exponential dependency of drive current on threshold voltage limits its application area. Hence there is pressing need to overcome

these limitations by device technology parameter optimization or selecting operating point of the device where both energy and speed are in acceptable range. Our proposed strategy is to design energy efficient and moderate performance 1-bit full adder in moderate inversion region (MIR) [4], where devices are operated at or near their threshold voltage to extend the application domain of subthreshold circuits. Moreover, in the moderate inversion region (MIR), the transistor exhibits performance close to subthreshold with much lower variability.

This paper presents an optimized static 1-bit full adder cell using fin field effect transistor (FinFET) [5], [6] and carbon nanotube field effect transistor (CNFET) [7]–[10] in the moderate inversion region (MIR) for achieving high energy efficiency, robustness and good performance. The operation in MIR region helps to recover the huge penalty in performance and also to minimize the energy/switching by optimum selection of important process parameters like oxide thickness and fin thickness for FinFET and number of carbon nanotube, chirality vector and pitch for CNFET. Moreover, it also performs variability analysis of the full adder circuit against process, voltage, and temperature (PVT) variations. Full adder based on emerging technologies like FinFET and CNFET are more robust than the conventional MOSFET-based full adder. It is a first attempt to the best of our knowledge to investigate the near threshold performance of a full adder cell in emerging technologies beyond CMOS. The full adder cells are analyzed and compared at 100 MHz on HSPICE environment using 32 nm BPTM (Berkeley Predictive Technology Model (BPTM) [11]. The results of CNFET-based full adder are based on the experimentally validated Stanford model [12]. The rest of the paper is organized as follows. Section II briefly describes the structure of the full adder cell. The FinFET structure is described in Section III. Section IV details the CNFET structure. The performance of full adder cell in different technologies is reported in Section V. Section VI explains the process parameter optimization of FinFET. Process parameter optimization of CNFET is reported in section VII. Section VIII presents comparison of full adder cells using optimized process parameters. Impact of PVT variations on design metrics is investigated in Section IX. Section X concludes this paper.

II. THE 1-BIT FULL ADDER CELL

The full-adder [13] operation can be described as follows: given the three inputs A, B, and C_{in} , it is desired to obtain two 1-bit outputs, SUM and CARRY, where

$$SUM = A \oplus B \oplus C_{in} \quad (1)$$

$$CARRY = A.B + C_{in} \times (A \oplus B). \quad (2)$$

Several logic styles are used in the literature to design full adder cells. Each design style has its own merits and demerits. Classical designs of full adders normally use only one logic style for the whole full-adder design. One example of such design is the standard static CMOS full adder shown in Fig. 1. This full adder is based on regular CMOS structure with conventional pull-up and pull-down transistors offering full-swing output and good driving capabilities.

III. FINFET STRUCTURE

Geometric parameters of the conventional Si-CMOS devices have been scaled down aggressively to achieve increased integration density, increased operational frequency and reduced power consumption. However beyond submicron region increased static leakage power dissipation and increased sensitivity to process variation in performance parameters cause major bottleneck for further device scaling. Researchers have shown that the promising multi-gate transistor [15] offers remarkable advantages in terms of different design metrics. It increases the driving current with the sub-threshold and gate tunneling leakage currents within acceptable limit as compared to the standard single-gate MOSFETs. The multiple electrically coupled gates and the thin silicon body suppress the short-channel effects (SCE), hence reducing the subthreshold leakage current in a multi-gate MOSFET. Reduced SCE improves subthreshold slope and allows increasing the oxide thickness which results in lower gate leakage current. It has been also observed from the previous research that multi-gate devices shows better parameters variation immunity than conventional single gate device. The most promising multi-gate device is the FinFET [5], [6] due to the self alignment of the two gates and the relative compatibility with the existing standard CMOS fabrication process. The architecture of a double-gate FinFET with symmetric gates is shown in Fig. 2. The fin thickness and the gate oxide thickness are the most significant dimensions in the design of FinFETs because these parameters have strong impact on its electrical characteristics [5].

IV. CNFET STRUCTURE

Most of the fundamental limitations for traditional silicon MOSFETs are mitigated in carbon nanotube field effect transistor (CNFET) shown in Fig. 3. With ultralong (1 micrometer) mean free path for elastic scattering, a ballistic or near-ballistic transport is obtained with an intrinsic carbon nanotube (CNT) under low voltage bias to achieve the ultimate device performance [7]–[10]. The quasi-1-D structure provides better electrostatic control over the channel region than 3-D device (e.g., bulk CMOS) and 2-D device (e.g., fully depleted SOI) structures [10]. Ballistic transport operation and low I_{OFF} (OFF-current) make the CNFET a suitable device for high performance and increased integration. The CNFETs can be scaled down to 10 nm channel length and 4 nm channel

width, thus providing a substantial performance and power improvement compared to the Si-MOSFET [14].

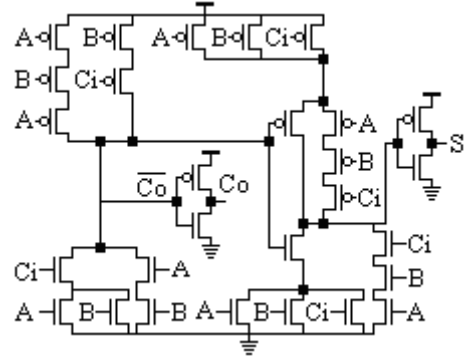


Figure 1. Standard CMOS 1-bit full adder cell with conventional MOSFET [13].

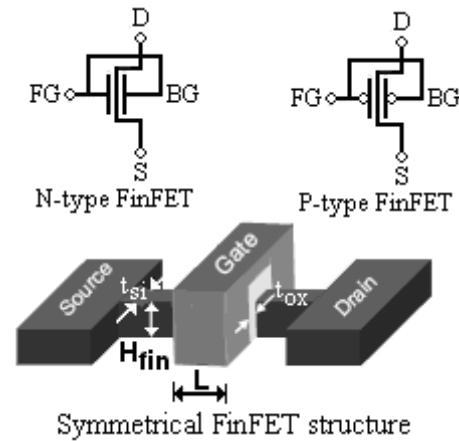


Figure 2. N-type FinFET, P-type FinFET and symmetrical FinFET structure. L: gate length. t_{si}: fin thickness. H_{fin}: fin height. t_{ox}: oxide thickness [5].

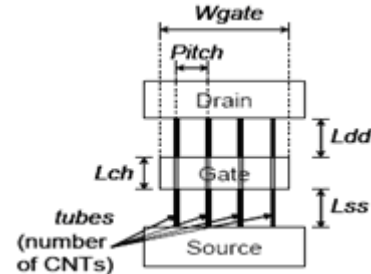


Figure 3. Top view of CNFET structure with multiple channels [12].

A single walled CNT (SWCNT) is formed by rolling a sheet of graphene (single atomic layer of graphite) into a cylinder. The direction of rolling, defined as chirality vector (n_1, n_2), determines the properties of the CNT as shown in Fig. 4. A CNT acts as a metal if $n_1 = n_2$ or $n_1 - n_2 = 3i$, where 'i' is an integer. Otherwise, the CNT is semiconducting. The V_t (threshold voltage) of CNFET can be varied with CNT diameter. The V_t of CNFET is an inverse function of the CNT diameter [14]. Compared to silicon technology, the CNFET shows better device performance than the Si-MOSFET even with device non-idealities. Increasing the number of CNTs per device is the most effective way to improve the circuit speed. Compared to Si-CMOS circuits, CNFET circuits with

one to ten CNTs per device is about two to ten times faster, the energy consumption per cycle is about seven to two times lower and the EDP (energy-delay product) is about 15–20 times lower [14].

V. PERFORMANCE OF FULL ADDER CELL IN DIFFERENT TECHNOLOGIES WITH NOMINAL PROCESS PARAMETERS

Nominal process parameters of FinFET- and CNFET-based designs are tabulated in Table I and II respectively. The 1-bit static CMOS full adder cells are analyzed with different supply voltages above the threshold voltage operating at a frequency of 100 MHz. The structure is simulated with a load capacitance of 50 fF and at a temperature of 50°C with minimum size transistors. The minimum size transistors are chosen to minimize the area and observe the severity of process variation. The BPTM (Berkeley Predictive Technology Model) used for MOSFET is the 32 nm high-performance, strained silicon, high-k metal gate model, which is used in Intel's latest silicon process technology. As transistors shrink and threshold voltage scales, leakage current increases exponentially. Managing that leakage is crucial for reliable low-power operation and is an increasingly important factor in circuit design. The gate leakage is significantly reduced in the high-k metal gate process used here for bulk CMOS giving rise to energy efficient and high performance systems. The proposed implementation in FinFET and CNFET technologies makes full adders even more energy efficient, robust and faster. This paper proposes the implementation of full adder (Fig. 1) using FinFET and CNFET technologies by replacing all the N-type MOSFET and P-type MOSFET with N-type and P-type FinFET/CNFET structures. The threshold voltages for all technologies are considered similar at nominal process parameters and also at the optimum process parameters for fair comparison. The PDPs of full adders are estimated by scaling V_{DD} (supply voltage) from 0.9 V down to 0.3 V (Fig. 5). It is apparent from Fig. 5 that for an input frequency of 100 MHz, the minimum energy point for the full adder cell using MOSFET and FinFET technologies is at $V_{DD} = 0.3V$. For MOSFET and FinFET-based full adders, the PDP decreases with decreasing V_{DD} . This is attributed to the fact that $P_{dynamic}$ (dynamic power) is quadratically related to V_{DD} . The $P_{dynamic}$ is the dominant contributor to the total energy consumption. However, for CNFET-based full adder, the PDP does not decrease as the supply voltage is scaled down in the similar manner. This so happens because at the nominal process parameters of CNFET,

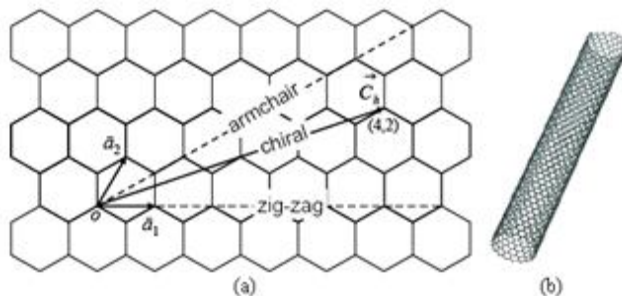


Figure 4. Lattice structure of (a) unrolled and (b) rolled graphite sheet to form CNT [14].

TABLE I. NOMINAL PROCESS PARAMETERS OF FINFET-BASED DESIGN

Parameter	Value
Supply Voltage(V_{DD})	0.9 V
Gate length(L)	32 nm
Fin height(H_{fin}) for N-FinFET	32 nm
Fin height(H_{fin}) for P-FinFET	64 nm
Fin thickness(t_{fin})	8.6 nm
Oxide thickness(t_{ox})	1.6 nm
Channel doping concentration	$2 \times 10^{16} \text{ cm}^{-3}$
Polysilicon gate doping concentration	$2 \times 10^{20} \text{ cm}^{-3}$
Threshold voltage for N-FinFET	0.29V
Threshold voltage for P-FinFET	-0.25V

TABLE II. NOMINAL PROCESS PARAMETERS OF CNFET-BASED DESIGN

Parameter	Value
Supply Voltage(V_{DD})	0.9 V
Gate length(L)	32 nm
Width of metal gate for N-CNFET	6.4 nm
Width of metal gate for P-CNFET	6.4 nm
Thickness of high-k-top gate dielectric material (t_{ox})	4.0 nm
Mean free path in intrinsic CNT	200 nm
Distance between the centers of two adjacent CNTs within the same device (Pitch)	20.0 nm
Chirality of tube	(19, 0)
Number of tube in the device.	1

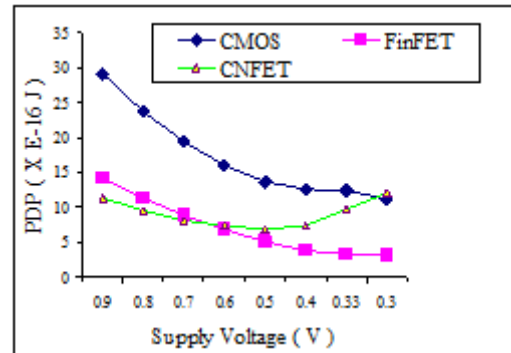


Figure 5. Power-delay product of full adders vs. V_{DD} at $f = 100$ MHz.

the delay increases at a faster rate than the reduction in power dissipation due to low driving capability of CNFET (since only one CNT is used for this design). Extensive simulation using HSPICE is carried out to establish the optimum V_{DD} and found that 0.33 V is the optimum operating voltage in the moderate inversion region (MIR) for the full adder cell using MOSFET and FinFET (keeping all design metrics in consideration). Although, the CNFET-based full adder in MIR does not offer minimum energy point, however minimum energy point is achieved by the optimum selection of most important process parameters even in case of CNFET. This supply voltage has been chosen to minimize the effect of delay penalty. Supply voltage variation of 10% is also considered. It is observed from Fig. 6 that FinFET-based full adder cell consumes higher power dissipation than the conventional MOSFET cell at all supply voltages due to its higher driving current [5], [6]. Although the leakage power dissipation for the FinFET structure is less than the single gate MOSFET structure, however increase in dynamic power dissipation is higher than the reduction in leakage power dissipation. The CNFET-based full adder cell has less power dissipation than FinFET structure with nominal process

parameters; this is because of lower driving current and capacitance values. It is observed from Fig. 7 that the full adder cell with FinFET has shorter delay than the conventional MOSFET cell at all supply voltages due to its higher current driving capability [5], [6]. The CNFET based full adder cell offers longer delay than the FinFET structure; this is because of lower current driving capability at the nominal process parameters. In the next section, the performance of FinFET-based adder is enhanced by optimization of FinFET's process parameters.

VI. FinFET's PROCESS PARAMETER OPTIMIZATION

The PDPs of FinFET-based full adder cell for different oxide thicknesses are shown in Fig. 8. PDP increases as the gate oxide thickness increases; this is because the reduction in power dissipation is less than the increase in delay. It is evident from Fig. 8 that the oxide thickness of 2.3 nm gives the optimum result for different performance parameters under consideration. The optimum value of the oxide thickness is then used to investigate the variation of PDP with fin thickness. The PDPs of the FinFET based full adder cell at different fin thicknesses is shown in Fig. 9. It is evident from Fig. 9 that the PDP decreases upto a certain value of fin thickness and then increases. It is clear that the fin thickness of 14 nm together with oxide thickness of 2.3 nm gives the optimum result for different performance parameters under consideration. In the next section, the performance of CNFET-based full adder is improved by the optimization of CNFET's process parameters.

VII. CNFET's PROCESS PARAMETER OPTIMIZATION

The PDP of the CNFET-based full adder cell for different number of carbon nanotubes is shown in Fig. 10.

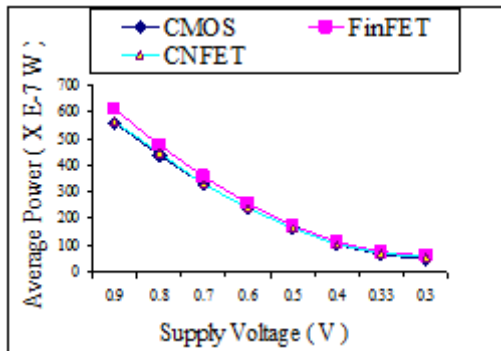


Figure 6. Power dissipation of full adder vs. V_{DD} at $f = 100$ MHz.

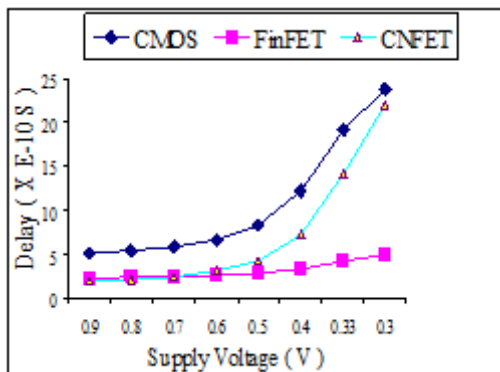


Figure 7. Delay of the full adder vs. V_{DD} at $f = 100$ MHz.

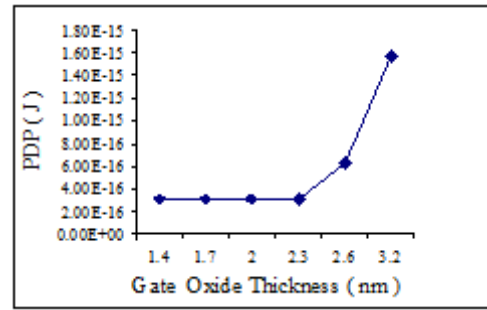


Figure 8. PDP of the FinFET-based full adder vs. oxide thickness.

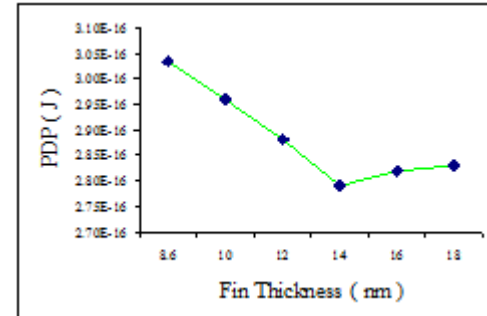


Figure 9. PDP of the FinFET-based full adder cell vs. fin thickness.

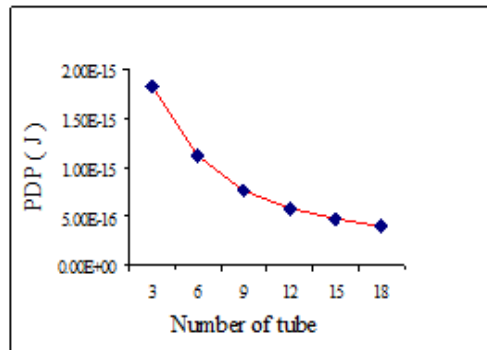


Figure 10. PDP of the CNFET-Based full adder cell vs. number of CNT.

It is observed from Fig. 10 that the PDP decreases with increase in number of CNT. This is due to the increase in the driving current and hence reduction in delay, which outweighs the increase in power dissipation. However, increase in number of CNT also incurs penalty in power dissipation and area. Thus, keeping all the design metrics (such as leakage, power, delay, and PDP) in mind the optimum number of CNT is chosen to be equal to 9. The optimum value of number of carbon nanotube is then used to observe the effect of chirality vector variation on the PDP. The PDP of the CNFET-based full adder cell at different chirality vector is shown in Fig. 11. It is observed from Fig. 11 that PDP decreases with increase in chirality vector. This occurs because V_t of CNFET decreases with increase in chirality vector resulting in decrease in delay and increase in power dissipation. The reduction in delay outweighs the increase in power dissipation. Hence, the PDP decreases with increase of chirality vector but at the cost of higher power dissipation. Thus, considering all design metrics like leakage and power, delay and PDP, chirality vector of (26, 0) is chosen to be optimal. The optimum value of chirality vector is then used to observe the effect of pitch variation on the PDP. The PDP of the CNFET-

based full adder cell at different pitch value is shown in Fig. 12. It shows that the PDP increases with decrease in pitch. This occurs because a decrease in inter-tube distance results in the reduction of drive current due to increase in inter-tube coupling. The decrease in drive current increases the delay. However, power dissipation decreases due to reduction in drive current. The increase in delay is higher than the reduction in power dissipation. Hence, the PDP increases with decrease in pitch. However, increase in pitch also incurs penalty in power dissipation. Therefore, keeping all design metrics in mind, a pitch of 20 nm is chosen to be the best that gives the optimum results together with optimum value of number of CNT and chirality vector. The performance and comparison of the adder cell in optimized technologies are described in the next section.

VIII. COMPARISON OF FULL ADDER CELLS USING OPTIMIZED PROCESS PARAMETERS

Different performance parameters using CMOS technology and technology beyond CMOS are reported in Table III. The values of average power, delay and PDP are normalized with respect to that of OP-CNFET (optimized CNFET-based full adder) and are reported in bracket. It is observed that the full adder cell with FinFET and CNFET technologies for optimum values of process parameters result in significant performance improvement. At the optimum value of process parameters, CNFET-based full adder has lowest power dissipation. This is due to the fact that the increase in its leakage power dissipation is much less than the full adder cell using MOSFET and FinFET structure, which is the dominant contributor to total power dissipations in the deep submicron regime. An improvement in delay is because of higher driving current of FinFET and CNFET technologies at the same supply voltages. It is apparent that the OP-FinFET (optimized FinFET-based full adder) consumes higher power dissipation than the conventional MOSFET-based full adder at all supply voltages. This is attributed to fact that FinFET has higher drive current [5], [6] at the same supply voltages due to the presence of its double gate. Although the leakage power dissipation of FinFET structure is less than single gate MOSFET, the increase in dynamic power dissipation is higher than the reduction in leakage power dissipation.

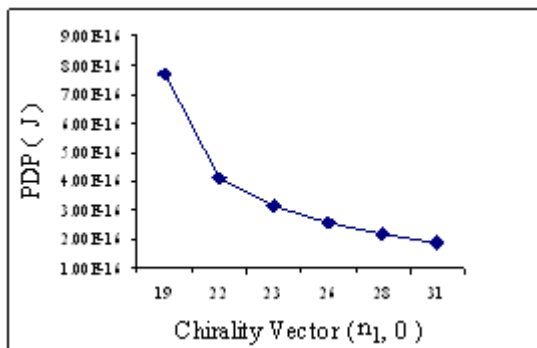


Figure 11. PDP of CNFET-based full adder cell vs. chirality vector

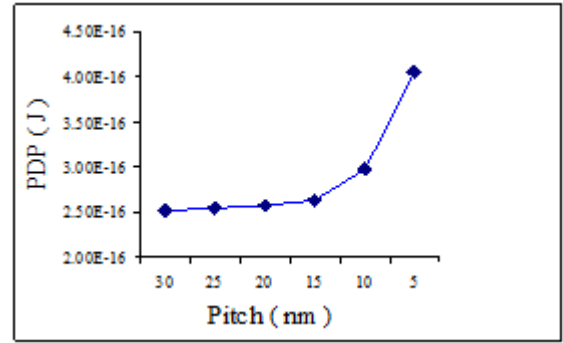


Figure 12. PDP of CNFET-based full adder vs. pitch.

TABLE I. COMPARISON OF FULL ADDER CELL USING OPTIMIZED PROCESS PARAMETERS AT $V_{DD}=0.33$ V

Full Adder Cell	Power ($\times 10^{-7}$ W)	Delay ($\times 10^{-16}$ s)	PDP ($\times 10^{-16}$ J)
CMOS	7.71(1.06)	11(3.13)	8.51(3.31)
OP-FinFET	9.78(1.34)	3.97(1.13)	3.88(1.51)
OP-CNFET	7.31(1)	3.51(1)	2.57(1)

There is an improvement in PDP also, since reduction in delay outweighs the increase in power dissipation. For the FinFET-based full adder cell, we conclude that fin thickness of 14 nm and gate oxide thickness of 2.3 nm together with supply voltage of 0.33 V gives the optimum result. For the CNFET-based full adder cell, we conclude that the number of CNT of 9, chirality vector of (26, 0), and 20 nm pitch together with supply voltage of 0.33 V gives the optimum result. The optimization of the full adder in terms of speed and power consumption is necessary to investigate the potential of technologies beyond CMOS. Its robustness against PVT variations is even more important and essential in deep submicron technology. The next section describes investigation of PVT variation for different technologies.

IX. INVESTIGATION OF IMPACT OF PVT VARIATIONS ON DESIGN METRICS

Due to aggressive scaling, random variations in process, supply voltage and temperature (PVT) are posing a major challenge to high performance circuits and system design [16]. The process variations include variation in oxide thickness (t_{ox}), channel length (L) in short channel devices, channel width (W) in narrow channel devices, substrate doping concentration (N_{SUB}), channel doping concentration (N_{CH}), polysilicon gate doping concentration (N_{POLY}), source/drain sheet resistance (R_{SD}). All these process parameters affect V_t , which in turn modulates the drain to source current I_{DS} . Therefore, propagation delay (t_p) along with average power dissipation (P) and power-delay product (PDP) are taken as important design metrics for the analysis and design of full adder circuit in this paper. PVT variations can be mitigated by various design techniques. Adaptive body biasing is one such technique [17]. Circuit design techniques such as body biasing will help, but their effect diminishes with technology scaling. This paper investigates for the first time to the best of our knowledge static CMOS 1-bit full adder against PVT variations at 32 nm technology node using Monte Carlo method in the moderate inversion region. This investigation

reveals the robustness of FinFET- and CNFET-based adder cell against PVT variations in the moderate inversion region. Device parameters t_{ox} , L , W , N_{SUB} , N_{CH} , N_{POLY} , R_{SD} are assumed have independent Gaussian distributions with 36 variation of 10% [6]. The values of average power, delay and PDP variability are normalized with respect to that of OP-CNFET and are reported in bracket (Table IV). It is observed from Table IV that the emerging technology-based full adder cells OP-FinFET and OP-CNFET offer tighter spread in power, delay and PDP variabilities against PVT variations. OP-FinFET full adder cell is more robust than the CMOS-based full adder cell because the short channel and process variation effects are minimized due to the presence of double gate in FinFET. Moreover, FinFET offers better channel electrostatic than MOSFET. It is observed that the CNFET is more robust against process variations compared to Si-CMOS. This is due to its cylindrical geometry. A variation in the gate oxide thickness that strongly affects the drive current and capacitance of CMOS transistors has a negligible impact on the CNFET operation. Moreover the gate width in CNFET is not the effective channel width of the transistor.

TABLE I. VARIABILITY ANALYSIS RESULTS OF FULL ADDERS USING CMOS AND TECHNOLOGIES BEYOND CMOS AT $V_{DD}=0.33$ V

Full Adder Cell	% Variability (σ/μ)		
	Power	Delay	PDP
CMOS	8.77(1.29)	14.45(2.54)	10.57(2.20)
OP-FinFET	7.07(1.04)	10.66(1.88)	5.14(1.07)
OP-CNFET	6.82(1)	5.68(1)	4.81(1)

X. CONCLUSION

This paper presents a technology beyond CMOS-based full adder cell optimized in terms of overall power, delay, and energy efficiency by judicious selection of process parameters and supply voltage. FinFET-based full adder cell is found to exhibit higher switching speed and energy efficiency as compared to MOSFET-based full adder cell in the Moderate Inversion Region (MIR) with nominal value of process parameters. The optimized FinFET-based full adder offers better performance and tighter spread in power consumption, delay and PDP against PVT variations. At nominal process parameters, CNFET-based full adder does not offer much improvement in different design metrics in the moderate inversion region. However for the optimum value of process parameters, it achieves the highest improvement in all the design metrics among all technologies considered in this paper. Moreover, the CNFET-based full adder cell exhibits more robustness against PVT variations than the MOSFET-based full adder cell. It is concluded that both the FinFET and CNFET technologies are very promising for realizing robust circuits such as full adder in future scaled technology nodes.

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Aminul Islam (M'10) graduated in Computer Engineering from The Institution of Engineers (India) in 2001, and post graduated in Electronics and Communication Engineering from Birla Institute of Technology (deemed university), Mesra, Ranchi, Jharkhand, India in 2006. Until November 2006, he was with Indian Air Force. Since November 2006, he has been with the Electronics and Communication Engineering Department, Birla Institute of Technology, Mesra, Ranchi, Jharkhand, India, where he is currently an Asst. Professor. His research interests include VLSI design for nanoscale emerging silicon and non-silicon technologies (that includes FinFET, CNFET), robust design of ultra-low power nanoscale circuit for portable computing and wireless communications. He is currently working toward the Ph.D. degree in the field of VLSI design from the Department of Electronics Engineering, Aligarh Muslim University, Aligarh, Uttar Pradesh, India. He has published more than 25 research papers in reputed Conferences and Journals.



Md. Waseem Akram received the B.Tech. degree in Electronics and Tele-Communication Engineering from National Institute of Science and Technology (NIST), Orissa, India in 2008, the M.Tech (Electronic Circuits & Systems Design) degree from Aligarh Muslim University, India in 2010. He is currently working toward the Ph.D.

degree from IIT, Kanpur, India in the Electrical Engineering Department. His research interests include computer-aided design for conventional nanoscale Silicon and non-conventional Silicon technologies (that includes FinFET, CNFET), robust design of ultra-low power nanoscale circuit for portable computing and wireless communications. He has published more than 10 research papers in reputed Conferences and Journals.



Dr. Mohd Hasan (M'10) received the B.Tech. degree in Electronics Engineering from Aligarh Muslim University (AMU), India in 1990, the M.Tech. degree in Integrated Electronics and Circuits from the IIT, Delhi, India in 1992 and joined as Lecturer in Electronics Engineering Department of AMU in 1992. He re

ceived the Ph.D. degree from the University of Edinburgh, UK in 2004 on a Commonwealth Scholarship in the area of Low Power Architectures for Multi-carrier Systems. He has also worked as a postdoctoral visiting researcher on a prestigious Royal Academy of Engineering, UK funded project on Low Power FPGA Architecture in 2008-2009 in the School of Engineering, University of Edinburgh, UK. He has been currently working as Professor at Aligarh Muslim University, Aligarh, India since 2005. He has published more than 100 research papers in reputed Journals and Conferences. His research interest includes Low power VLSI design, Nanoelectronics, FPGA Architectures along with Embedded System Design.